MBEF

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
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Robert Lester Kenneth Chin Jım Blocker John Larson

Internal control bus in a multiple processor/multiple bus system

TITLE

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ORIGINAL			CROSS R	EFERENCE	(S)	1.1:44 4	功用数
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TERMINAL	DRAWINGS		CLAIMS ALLOWED				
DISCLAIMER	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.		
The term of this patent				NOTICE OF ALL	OWANCE MAILED		
subsequent to (date)			·	·			
has been disclaimed.	(Assistant	Examiner)	(Date)		1		
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	(Legal Instrum	ents Examiner)	(Date)	ISSUE BAT	TCH NUMBER		

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